AMENDMENTS TO THE DRAWINGS

The attached drawings include changes to Figure 2 adding reference numbers of client ports.

Four (4) pages of replacement formal drawings are being submitted and replace any previous drawings submitted.

Attachment: Annotated Sheet Showing Changes
Replacement Sheets

REMARKS/ARGUMENTS

Claims 1-17 are pending in the application.

Applicants thank the Examiner for withdrawing the finality of the last Office Action.

The Examiner has asked Applicants to mention "client ports" in the title. Applicants respectfully decline. Applicants agree with the Examiner that the title should be indicative of the invention to which the claims are directed. However, "distributed caches" are what the claimed invention is directed to and what distinguishes the claimed invention from the prior art, and they are already mentioned in the title. A "client port" is only used to couple a sub-unit cache and a port component, and is not what the claimed invention is directed to.

The Examiner has objected to the drawings. Applicants have added reference numbers of client ports in Fig. 2 and the specification. A skilled artisan should appreciate where the client ports are in Fig. 2 from the original disclosure. No new matter has been introduced.

Applicants have corrected some informalities in claim 9, as the Examiner has suggested.

Claims 1-4, 6-12 and 14 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,629,213 to Sharma. Applicants respectfully disagree.

Sharma is about an apparatus for accessing a segment of data, which is less than the size of a cacheline, from a main memory. As shown in Fig. 1 of Sharma, a computer system 100 has a number of cells 102. Each cell includes a number of processors 106 connected to a memory controller unit 108. The memory controller unit 108 is also connected to a memory bank 112 and an I/O subsystem 114, and controls access to the system memory. An I/O subsystem includes an I/O bridge unit 116 connected to a number of I/O devices 122 through a bus 120. The I/O bridge unit 116 includes one or more cache units 118, and the cache units 118 are

connected by a local communication link 124, and are connected to the memory controller unit 108. Each cache unit 118 is also connected to one or more buses 120 that are coupled to one or more I/O devices 122. As shown in Fig. 2 of Sharma, the cache unit 118 includes a cache controller unit 150 that is connected to a cache 152 through a local communication link 154 (Sharma, col. 1, line 56 to col. 3, line 52).

Claim 1 is directed to a cache-coherent input/output device including a plurality of sub-unit caches, each assigned to one of a plurality of port components; and a coherency engine coupled to the plurality of sub-unit caches.

The Examiner has read the recited plurality of sub-unit caches on cache units 118 in Sharma, has read the recited plurality of port components on I/O devices 122 in Sharma, and has asserted that Sharma teaches assigning each of the plurality of sub-unit caches to one of said plurality of port components. However, in Sharma, each cache is connected to one or more PCI buses 120 that are coupled to one or more I/O devices 122 (Sharma, col. 3, lines 42-44). In Fig. 1 of Sharma, each cache unit 118 is connected to four I/O devices 122. There is no disclosure in Sharma that any particular I/O device 122 is assigned to any particular cache unit 118. Thus, Applicants respectfully submit that Sharma fails to teach assigning each of the plurality of sub-unit caches to one of a plurality of port components.

It appears that the Examiner has read the recited coherency engine on both the memory controller 108 and cache controller unit 150. However, the memory controller 108 is not a part of the I/O system in Sharma. In Sharma, the I/O system 114 includes an I/O bridge unit 116 connected to a number of I/O devices 122 though a bus 120 (Sharma, col. 3, lines 23-25), but not the memory controller unit 108.

Further, the cache controller unit 150 only controls operation of one individual cache unit. Nothing in Sharma indicates that the cache controller unit 150 in one cache unit is coupled to other cache units. In Sharma, each cache unit 118 has a cache controller unit 150 that is connected to a cache 152 through a local communication link 154 (Sharma, col. 3, lines 48-51). When processing a DMA read request, the cache controller unit 150 will receive a DMA read request from an I/O device 122 at step 180, and requests from the memory controller unit 108 a copy of the requested bytes at steps 188 or 190. When the requested bytes are returned to the cache controller unit 150, the data is placed in the cache 152 of the cache unit 118, and sent to the requesting I/O device 122 at step 194 (Sharma, col. 5, lines 15-67, and Fig. 4). When processing a DMA write request, the cache controller unit 150 obtains ownership of data by transmitting a command to the memory controller unit 108 at step 248 or 252 (Sharma, Fig. 7). Thus, the cache controller unit 150 only controls the data transfer between the memory controller unit 108 and one I/O device 122.

Accordingly, Applicants respectfully submit that Sharma fails to teach the coherency engine in claim 1.

From the foregoing, Applicants respectfully submit that claim 1 and its dependent claims 2-5 are patentable over Sharma. Claims 6-8 are patentable over Sharma for similar reasons.

Claim 9 recites the feature "each of the sub-unit caches assigned to one of a plurality of client port". As discussed above, Sharma fails to teach or suggest this feature. Accordingly, Applicants respectfully submit that claims 9-17 are patentable over Sharma.

Claims 5, 13, and 15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over

Sharma in view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp 140-240.

Handy discloses a protocol for use in multiple processor system with multiple caches, and fails to supply any deficiency of Sharma. Accordingly, Applicants respectfully submit that claims 5, 13 and 15 are patentable over the combination of Sharma and Handy.

Claims 16-17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma, in view of Handy, and further in view of U.S. Patent 6,202,139 to Witt.

Witt discloses a computer system including a processor having a cache which includes multiple ports. The cache is pipelined and operates at a clock frequency higher than that employed by the remainder of the microprocessor including the cache for multiple accesses per clock cycle (Witt, col. 2, lines 31-36 and Abstract). Thus, Witt does not supply any deficiency of Sharma or Handy. Accordingly, Applicants respectfully submit that claims 16 and 17 are patentable over the combination of Sharma, Handy and Witt.

For all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to the deposit account of Kenyon & Kenyon LLP, deposit account no. **11-0600**.

Respectfully submitted,

KENYON & KENYON LLP

Dated: March 5, 2007

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CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this paper is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 5, 2007.

Monique Cruz

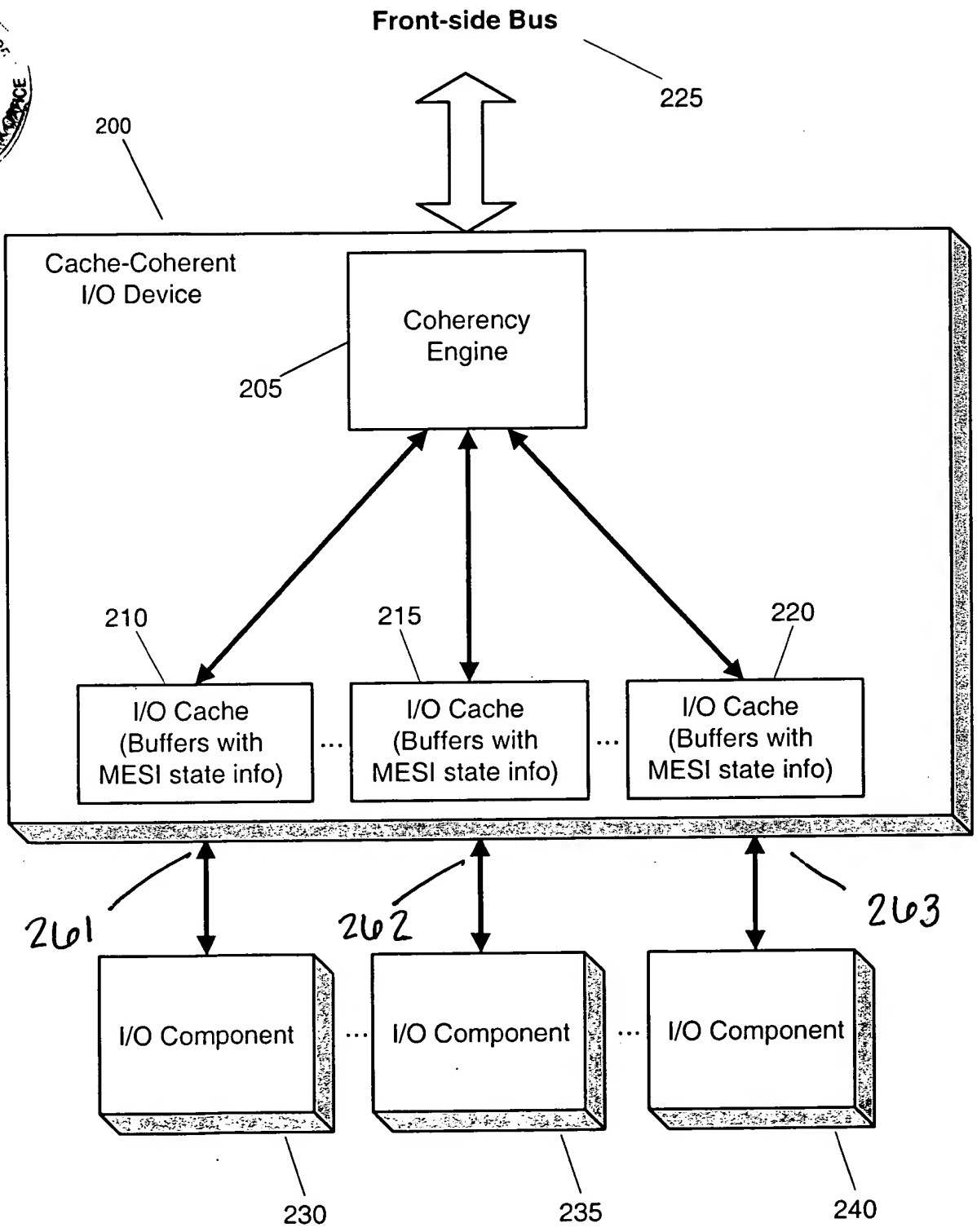

Fig. 2